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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/845,752	04/25/97	SHRIVASTAVA R	B-5500

EXAMINER	
CRANE,S	
ART UNIT	**PAPER NUMBER**
2811	

MM92/1114

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DATE MAILED:
11/14/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/845,752	Applicant(s) Shrivastava et al.
	Examiner Sara W. Crane	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Aug 28, 1900* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-22, 24, 26-34* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-22, 24, 26-34* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Lee.

With respect to claim 1, figures 1A and 1B of Sung et al. show each feature claimed. *First of all, rotate the figure by 90 degrees, so that the long side of the page extends left to right.* Figure 1B shows a plurality of memory cells, each cell defined by a drain region D (40), a source region (S in figure 1A) under source line 40', a channel area between source and drain, a floating gate 12, and a control gate 14. Each source and each drain are shared between adjacent cells. In figure 1B, *after it has been rotated by 90 degrees*, each conductive member 40' is disposed along a portion of a row, and the drain regions are arranged in two columns, one on the left having three drain members 40, and one on the right having three drain members 40. The conductive member 40' makes contact with the source regions of the member cells of the portion of the row as shown. The conductive member 40' is self-aligned with each of the memory cells in the row, because alignment occurs automatically when layer 40' is deposited between sidewall regions 29'. It would have been obvious to rotate the page of figures 1A and 1B by 90 degrees because one of ordinary skill would know that device orientation does not affect device function, and because in use the

device could be oriented in any way at all. Alternatively, Lee shows source lines 160 in figure 19 running from top to bottom of the page, and these are called "rows" (column 7, lines 36-38).

With respect to claims 2-3, figure 1B shows conductive member 40' contacting a row of source regions, where each source region is shared by memory cells on each side of conductive member 40'.

With respect to claim 4, the control gates 14 of the Sung device would have to be commonly coupled to a word line, as discussed by Lee at column 1, lines 31 or column 2, lines 7-8.

With respect to claim 5, it would have been obvious to overlap the word lines with the source lines, as shown in the cover figure of Lee (where word lines 14 are overlapped by source lines 160), in order to allow for larger source lines having lower resistance.

With respect to claim 6, see the discussion of claims 2-5 above.

With respect to claim 7, it would have been obvious to make the source line of polysilicon as taught by Lee (abstract, line 7) because polysilicon provides low resistivity for device connections.

With respect to claims 8-9, Lee teaches to use tungsten silicide or polycide as the source line (column 4, line 43, and column 7, lines 33-36). It would have been obvious to used polycide for the Sung source lines as well, to obtain the lowered resistance of silicide. Tungsten is a metal.

Claims 10-22, 24, and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. and Lee in view of Wong et al.

With respect to claim 10, the cover figure of Wong et al. teaches a source line decoder and driving circuit for controlling voltages on the word line and the source line during erase (column 6, lines 59-62). It would have been obvious to provide a source line decoder and driving circuit as taught by Wong et al. to bias word lines and source lines in the Sung and Lee memory cells, because voltages on the word lines and source lines must be controlled during erase.

With respect to claim 11, Wong et al. teaches in the cover figure that source decode signals are generated in response to an address signal.

With respect to claim 12, computer memory is usually addressed for erase in response to user input at a keyboard.

With respect to claim 13, the cover figure of Sung et al. shows a first flash memory cell, second transistor from the left, where the top of the cell is at the top of layer 14, a first cell side would be at the right of layer 14, and a second cell second side opposite the first cell side. First insulating sidewall 28, 29' is formed on the first side of the first flash memory cell, and conductive member 40' is disposed on the first insulating sidewall and making contact with a contact portion of the substrate. As shown in figure 1B, each layer 40' is associated with a row of cells *(turn the page by 90 degrees)*. As shown by Wong et al., erasing of memory cells requires a voltage to be applied to a source line. Because a voltage can be applied to the Sung source line 40', it is possible to selectively erase the memory cells of a row aligned along the source line 40'.

With respect to claim 14, each of the Sung cells includes the layers recited.

With respect to claims 15-16, Lee motivates polysilicon and silicide for conductive lines, as noted above.

With respect to claim 17, Lee shows a second flash memory cell, third transistor from the left, having all structural features recited. Conductive member 40' is disposed on the sidewall of this second cell as well as on the sidewall of the first cell, because it is connected to the source region shared by the two cells. Because the source regions are shared by cells lying on both sides of conductive line 40', rows lying on both sides of this line can be erased simultaneously, or separately, depending on the voltages applied to the respective word lines.

With respect to claims 18-19, a common source region is shared by each of the adjacent Lee cells.

With respect to claim 20, see Sung et al. figure 1B (*rotate the figure by 90 degrees*).

With respect to claim 21, erasure takes place by applying a voltage to the source and the word line simultaneously, as taught by Wong et al. Because a voltage can be applied to one of the Lee source lines 40', without applying a voltage to other of the source lines 40', the Lee connections allow for selective erasing of the cells of one or more of the row pairs during an erase operation.

With respect to claim 22, the bit line contacts are the drain contacts.

With respect to claim 24, the word lines are the same as the control gates, as noted above, and the control gates of the Lee device would run parallel to the source lines 40'.

With respect to claims 26-29, source decoder and driver circuits are taught by Wong et al., and would be necessary to use the memory arrays of Sung et al. or Lee, as noted above.

With respect to claim 30, see Sung et al. figure 1B (*rotate the figure by 90 degrees*). An erase voltage applied between source line 40' and one of the adjacent word lines 14 would enable one of the two adjacent rows to be erased.

With respect to claims 31-34, each of the features is taught by Sung et al. or Lee as noted above.

Conclusion

Applicant's arguments filed with respect to the pending claims have been fully considered but they are not persuasive. Applicant argues that "the architecture disclosed by Sung et al. does not provide the capability of selectively erasing one or more rows of memory cells, since it does not teach source conductive members that are connected to the source regions of memory cells of adjacent roll pairs [row pairs?], and that are independent of each other." Sung et al. does teach source conductive members that are connected to the source regions of memory cells of adjacent rows, and that are independent of each other. See figure 1B. *Now rotate the figure by 90 degrees.* Each "source conductive member" 40' is connected to the source regions or memory cells in the adjacent rows. One row is immediately above line 40', and one row is immediately below line 40'. The row of cells above line 40' and the row of cells below line 40' are a row pair.

Each line 40' is associated with such a row pair, and each line 40' is independent from the other lines 40'.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (703) 308-4894.

The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 308-0956.

Sara W. Crane
Examiner
Art Unit 2811